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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,237	01/10/2006	Martin J. Edward	GB03 0112 US1	6993

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,237	EDWARD, MARTIN J.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 9 recites the limitation "the refresh circuit" in claim 9, line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8-9, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Aoki et al (6,307,532) hereinafter, Aoki.

5. In regards to claim 1, Aoki teaches an active matrix array (col. 9, lines 1-5), comprising: an array of matrix elements arranged in rows and columns (fig. 2 rows and columns), each matrix element comprising a circuit (fig. 2 120);

a plurality of column conductors (fig. 2 112), each arranged for inputting data signals to (col. 8, 30-43 Examiner notes because of the "or" operator it was not

necessary to examine the "outputting data signals"), the matrix elements of a respective column in first time periods and

means for providing power supply voltages for the circuit to the matrix element via the column conductors in first time periods interspersed between the first time periods (fig. 5 "Pre-charging signal PC" and "Pixel Data" col. 9-10, lies 65-14). Examiner notes during a pre-charging period power is sent down the data lines.

6. In regards to claim 12, Aoki teaches a method of operating an active matrix (col. 9, lines 1-5) array device comprising an array of matrix elements arranged in rows and columns (fig. 2 rows and columns), wherein each matrix element comprises a circuit requiring power supply voltages to be supplied to the circuit (fig. 2 120), the method comprising:

in first time periods inputting a data signal to (col. 8, 30-43 Examiner notes because of the "or" operator it was not necessary to examine the "outputting data signals"), the matrix element via column conductors and

in first time periods interspersed with the first time periods providing the power supply voltages to the circuit via the column conductors (fig. 5 "Pre-charging signal PC" and "Pixel Data" col. 9-10, lies 65-14).

7. In regards to claim 2, Aoki teaches an active matrix array wherein the means for providing power supply voltages for the circuit to the matrix element via the column conductors comprises, in each matrix element, differentiating means for operating differently according to whether the column conductors are being supplied with the power supply voltages or whether the column conductors are being supplied with the data signals (fig. 3 (114)). Examiner notes 114 is a switching element that offers means for operating differently according to an input col. 8, lines 44-62.

8. In regards to claim 3, Aoki teaches an active matrix array according to claim 1 (col. 9, lines 1-5), wherein the array further comprises means for receiving a control signal to the matrix elements (fig. 3 control signals from (20) to (172) and (106)), the control signal being such as to indicate to the matrix elements when the column conductors are being supplied with the power supply voltages and when the column conductors are being supplied with the data signals (fig. 2 signals from (20) Examiner notes that the control signals indicate by supplying either power or data signals); and wherein the differentiating means in each matrix element comprise means for operating differently in response to the control signal (fig. 3 (172) and (106) col. 11, lines 24-54).

9. In regards to claim 4, Aoki teaches an active matrix array according to claim 1 (col. 9, lines 1-5), wherein the matrix elements are pixels for a display device ("pixel" abstract); and each pixel comprises in addition to a respective one of the circuits, a pixel

electrode and a pixel select switching means coupled to the pixel electrode (fig. 3 114 and 116).

10. In regards to claim 5 Aoki teaches an active matrix array according to claim 4, wherein the circuit is a refresh circuit for refreshing the pixel electrode (col. 9, lines 8-30 and fig. 1 HYSNC). Examiner notes that picture is refreshed according to the horizontal synchronization pulse and the display starts to scan a new line and are applied to the circuit (fig. 2 (120)).

11. In regards to claim 6, Aoki teaches an active matrix array according to claim 3, wherein the pixels are adapted such that the control signal is used to indicate to the pixel when the column conductors are carrying the power supply voltages and to switch the pixel from a state where the pixel electrode receives picture data from the column conductors to a state where the pixel electrode receives inverted refresh picture data from the refresh circuit (fig. 3 (172) and (106) col. 11, lines 24-54).

12. In regards to claim 8, Aoki teaches an active matrix array of claim 3 wherein the means for receiving a control signal is coupled to the gate of a first control thin film transistor, TFT arranged to allow picture data to be provided to the pixel electrode only when the control signal is set such as to turn the first control TFT on (fig. 3 (106) col. 11,

lines 24-53). Examiner notes in fig. 5 Pre-charging signal is not on when the pixel data is sent.

13. In regards to claim 9, Aoki teaches an active matrix array according to claim 8, wherein the means for receiving a control signal is coupled to the gate of a second control TFT (fig. 3 (172)) arranged to allow refresh data to be provided from the refresh circuit to the pixel electrode only when the control signal is set such as to turn the second control TFT on and the first control TFT (fig. 3 (106)) off (fig. 5 Pre-charging signal and Pixel Data).

14. In regards to claim 11, Aoki teaches an active matrix array according to claim 1, wherein a first power supply voltage level is supplied to the circuits of a first column of matrix elements via a first column conductor arranged to also input or output data signals to or from the first column of matrix elements, and a second power supply voltage level is supplied to the circuits of the first column of matrix elements via a second column conductor arranged to also input or output data signals to or from a second column of matrix elements (fig. 2 PV1 and PV2 and fig. 9 and 10 + and -).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki, in view of Akiyama et. al (US 6,278,426) hereinafter, Akiyama.

18. In regards to claim 7, Aoki teaches using MOS transistor (col. 8, lines 65).

Aoki differs from the claimed invention in that Aoki does not explicitly disclose wherein the circuit comprises a CMOS inverter.

However, Akiyama teaches a system and method for wherein the circuit comprises a CMOS inverter (col. 11, lines 1-8).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Aoki to include the use of a CMOS inverter as taught by Akiyama in

order to reduce noise since CMOS are widely used for their ability for high noise immunity and low static power consumption.

19. In regards to claim 10, Aoki differs from the claimed invention in that Aoki does not disclose wherein the means for receiving a control signal is coupled to the gate of a third control TFT arranged to allow the power supply voltages to be supplied to the refresh circuit only when the control signal is set such as to turn the second and third control TFTs on the first control TFT off.

However, Akiyama teaches a system and method for wherein the means for receiving a control signal is coupled to the gate of a third control TFT (fig. 8 (206)) arranged to allow the power supply voltages to be supplied to the refresh circuit (col. 10, lines 20-40 of Akiyama).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Aoki to include the use of an active matrix array wherein the means for receiving a control signal is coupled to the gate of a second control TFT arranged to allow refresh data to be provided from the refresh circuit to the pixel electrode only when the control signal is set such as to turn the second control TFT on and the first control TFT off as taught by Akiyama in order to reduce the size and have one interconnect less than normal and improve light utilization efficiency as stated in (col. 10, lines 20-40 of Akiyama).

Aoki as modified by Akiyama teaches wherein the means for receiving a control signal is coupled to the gate of a third control TFT (fig. 8 (206) Aoki) arranged to allow

the power supply voltages to be supplied to the refresh circuit only when the control signal is set such as to turn the second and third control (fig. 8 (206) Aoki) TFTs on the first control TFT (fig. 3 (106)) off (fig. 5 Pre-charging signal and Pixel Data)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(6,911,964) Lee et al

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/G. D. S./
Examiner, Art Unit 2629
January 13, 2009